MPL3E

System on FPGA module

Based on a Xilinx Spartan-3E1200 or 3E1600 the MPL3E is ideal for building embedded systems with exactly the functions and interfaces needed.

Morphologic
Embedded FPGA Solutions
www.morphologic.dk

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Product key features:

The MPL3E module is a general purpose FPGA module intended for system-on-FPGA designs. The module contains the basic on-board components normally needed for embedded systems, such as high-speed DDR SDRAM, FLASH, SRAM, watch-dog and a power supply. The integration of the FPGA with the standard components on a module, significantly simplifies the design and multilayer PCB layout effort required to build a system on FPGA.

Building a system on a FPGA, allows the user to build the system as required in the system, which may include custom built functionality/interfaces as well as one or more microprocessors and functions/interfaces, such as UARTS, timers, II2/SPI controllers, GPIO ports, ethernet etc., commonly used in embedded systems. It also allows the system to be altered and even upgraded in the field, should new requirements arise during the product / product family lifetime. Building and integrating all the system functions onto a single module, simplifies the hardware design, reduces the BOM and makes it more robust.

Measuring only 49x61 mm (1.93x2.40”) the module connects to a base PCB using two quality 120-pin 0.8 mm pitch connectors, carrying the power and IO signals.

Module components:

- Xilinx Spartan 3E FPGA (2 sizes available: 1200 and 1600 kgates).
- 16 bit wide DDR SDRAM chip with up to 128 Mbytes capacity. 600 Mbyte/s burst bandwidth.
- 16 bit wide NOR FLASH with up to 128 Mbytes capacity.
- 16 bit wide low-power SRAM with up to 4 Mbytes capacity, with battery backup capability, allowing machine states to be stored and resumed during a power-failure.
- Supervisor chip for voltage supervision, backup voltage switching, reset generation and watch-dog function.
- Dual auto boot system: System will boot from backup FPGA image if the main image has been corrupted.
- 1.2 and 2.5V power supply circuitry with 3.3V input voltage. These voltages are available on the connector and can drive additional circuitry.
- Two 120-pin 0.8 mm pitch board-to-board connectors with 143 IO/I pins available from the FPGA as well as JTAG, power and 8-bit shared data bus.
- On-board 50 MHz oscillator.
- On-board LED indicators for: boot image selection, configuration status / user defined.

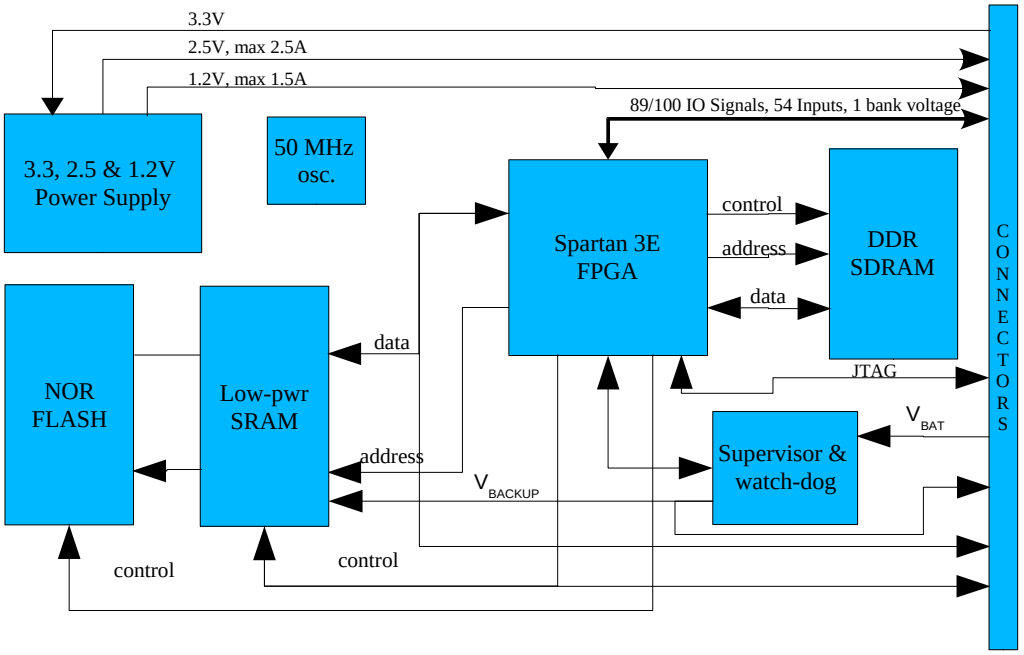
Typical FPGA functions:

- **Xilinx Microblaze processor**:
  - 32-bit Harvard architecture CPU running at frequencies up to 100 MHz.
  - Instruction and data cache using internal block-rams.
  - MMU option.
  - Floating point unit option.
  - Interrupt and exception capabilities
  - Efficient fast serial link interface for coprocessor functions etc.
  - Hardware shifter and multiplier.

- **Xilinx MPMC DDR SDRAM controller allowing high bandwidth DMA transfers.**
- **10/100 Mb/s Ethernet mac**
- **Display controller.**
- **Keyboard interfaces**
- **General purpose IOs**
- **Timer/counters**
- **Serial ports**
- **DMA controllers**
- **Storage media interfaces (IDE / CF / SDI interface)**
- **Custom logic:**
  - Special device interfacing
  - DSP processing
  - Coprocessor host interfacing
  - Telecom line interfacing
  - Motor controller (stepper, brushless etc.)
  - Image analysis (neural networks and other vision algorithms)
  - Hardware implemented control loops
- **Example applications**
  - Man Machine Interfaces with keyboard and graphics LCD screen.
  - Image analysis (neural networks and other vision algorithms)
  - Networking devices – media routers/ bridges.
  - Thin Clients
  - Industrial Controllers
  - Display controllers
  - Measuring instruments
  - Data acquisition and supervision units
  - Voice over IP units
  - DVB data processing
  - Motor controller (stepper, brushless etc.)

- **Supported operating systems (based on microblaze CPU):**
  - Linux
  - eCOS
  - AT Nucleus Plus
  - Micrium µC/OS-II
  - QNX Neutrino
  - Wind River VXWorks
  - Express Logic ThreadX
  - MontaVista LSP
  - Xilinx RTOS

Block Diagram:



Functional Description:

The MPL3E system on FPGA module is built around the Spartan-3E series of FPGA's. Supported devices are the XC3ES1200/1600 in the FGG320 BGA package using speed grade -4 or -5 (see ordering information). When using the Xilinx Microblaze processor, typical CPU clock frequencies of around 75MHz (-5 device) and DDR SDRAM clock speeds of 150 MHz are obtainable. Maximum clock speeds, speeds depend on the actual FPGA utilization, but is mainly determined by the number of devices on the internal buses. Other soft-core CPUs can be used on the board. Although the module architecture is targeting systems containing one or more CPU's, it can also be used for systems without a CPU.

FPGA

The FPGA is connected to the user IO, the DDR SDRAM, the NOR flash memory, the watch-dog and a 50 MHz oscillator. The configuration signals and JTAG buses are available on the connectors, allowing expansion of the system with more FPGA's and/or JTAG devices. FPGA's attached to the configuration signals can be configured from additional bit-images stored in the flash, eliminating the need for an extra configuration memory. The FPGA is supplied with 1.2V core voltage and 2.5 and 3.3V IO voltages. IO bank 2 and 3 operate on 3.3V IO, IO bank 3 operate on 2.5V while for IO bank 0, the IO voltage pins available on the connectors and is therefore user-selectable.

DDR SDRAM

The DDR SDRAM is connected to bank 3 of the FPGA and will support 16-bit devices with 13 address lines, currently up to 512Mbit (64 Mbytes). Maximum continuous burst transfer rate at 150 MHz is 600 Mbytes/s. Max. PLB bus bandwidth using 16 word bursts is in the range of 250-300 Mbyte/s.

NOR parallel flash

The non-volatile NOR based parallel flash chip is connected to the BPI (Byte Peripheral Interface) signals of bank 1 and 2 of the FPGA and will support devices from 16Mbits (2 Mbytes) to 1 Gbits

(128 Mbytes). Configuration of the FPGA is done automatically by reading configuration data from either the bottom (normal configuration) or the top of the flash (backup configuration). After configuration, the flash is available with a 16-bit wide data bus. Initial programming of the flash is done by downloading a boot loader or flash programming utility using the JTAG interface.

50 MHz oscillator.

The oscillator provides a stable 50 ppm precise 50 MHz clock. This clock can be fed internally to the DCMs in the FPGA, where other frequencies can be generated as needed.

Watch-dog, supervisor and battery switch-over

The watch-dog and supervisor IC is the maxim MAX6362P. At power-on the IC will generate a reset signal, which will pull down the PROG_B signal of the FPGA, When released the FPGA will start it's configuration sequence. The supervisors ICs watch-dog must then be triggered by the FPGA to avoid the watch-dog pulling low PROG_B again, causing a reconfiguration – this time from the top of the FPGA (backup image). When main power to the module is off, the supervisor chip will change to provide power to the SRAM via the battery backup voltage pin on the connectors.

Power Supply

The power supply uses a 3.3V supply to generate 1.2 and 2.5V system voltages. Both of these supplies are available on the module connectors. The 1.2V output will provide up to 1.5A and the 2.5V output will provide up to 2.5A. For most applications, this allows an external baseboard FPGA (or other devices) to be powered from the module supply, eliminating the need for extra power-supplies. The power supplies typically operates with an efficiency above 90%.

Module connectors

The module connectors are two JAE series KX15 120 pin 0.8mm pitch connectors. The default connector mounted is KX15-120K2DE. Other connector heights are available on special request. The pin configuration is given below:

Table 1: J2 connector pin out

Pin #	***Pin name***	***FPGA Pin name***	***FPGA Pin #***	***Description***
1	B3_I11	B3_IP13	U1	Bank 3, input only
2	B3_I10	B3_IP12	R1	Bank 3, input only
3	B3_I9	B3_IP11	N2	Bank 3, input only
4	B3_I8	B3_IP10	N1	Bank 3, input only
5	B3_I7	B3_IP9	M1	Bank 3, input only
6	B3_I6	B3_IP8	K7	Bank 3, input only
7	B3_I5	B3_IP7	K2	Bank 3, input only
8	B3_I4	B3_IP6	J7	Bank 3, input only
9	B3_I3	B3_IP5	G1	Bank 3, input only
10	B3_I2	B3_IP4	F5	Bank 3, input only
11	B3_I1	B3_IO_IP3	F4	Bank 3, input only
12	B3_I0	B3_IP2	D3	Bank 3, input only
13	GND			
14	GND			
15	B0_IO42	B0_IO_L24N	B4	Differential pair with B0_IO43
16	B0_IO45	B0_IO_L25P	C3	Differential pair with B0_IO44
17	B0_IO43	B0_IO_L24P	A4	Differential pair with B0_IO42

Pin #	*Pin name*	*FPGA Pin name*	*FPGA Pin #*	*Description*
18	B0_IO44	B0_IO_L25N /HSWAP	B3	Differential pair with B0_IO45, pulled to VCC_0 with 4.75Kohm
19	GND			
20	GND			
21	B0_I13	B0_IP_L22N	B5	Differential pair with B0_I14 (input only)
22	B0_IO40	B0_IO_L23N/ VREF	D5	Differential pair with B0_IO41
23	B0_I14	B0_IP_L22P	A5	Differential pair with B0_I13 (input only)
24	B0_IO41	B0_IO_L23P	C5	Differential pair with B0_IO40
25	GND			
26	GND			
27	B0_IO37	B0_IO_L20P	B6	Differential pair with B0_IO36
28	B0_IO38	B0_NC_IO_L 21N	E6	Differential pair with B0_IO39
29	B0_IO36	B0_IO_L20N	A6	Differential pair with B0_IO37
30	B0_IO39	B0_NC_IO_L 21P	D6	Differential pair with B0_IO38
31	GND			
32	GND			
33	B0_IO32	B0_IO_L18N/ VREF	D7	Differential pair with B0_IO33
34	B0_IO34	B0_IO_L19N/ VREF	E7	Differential pair with B0_IO35
35	B0_IO33	B0_IO_L18P	C7	Differential pair with B0_IO32
36	B0_IO35	B0_IO_L19P	F7	Differential pair with B0_IO34
37	GND			
38	GND			
39	B0_I11	B0_IP_L16N	D8	Differential pair with B0_I12 (input only)
40	B0_IO30	B0_IO_L17N	F8	Differential pair with B0_IO31
41	B0_I12	B0_IP_L16P	C8	Differential pair with B0_I11 (input only)
42	B0_IO31	B0_IO_L17P	E8	Differential pair with B0_IO30
43	GND			
44	GND			
45	B0_IO27	B0_IO_L14P/ GCLK10	C9	Differential pair with B0_IO26
46	B0_IO29	B0_IO_L15P	E9	Differential pair with B0_IO28
47	B0_IO26	B0_IO_L14N/ GCLK11	D9	Differential pair with B0_IO27
48	B0_IO28	B0_IO_L15N	F9	Differential pair with B0_IO29
49	GND			
50	GND			
51	B0_I10	B0_IP_L13/G CLK8	B8	Differential pair with B0_I9 (input only)
52	B0_IO22	B0_IO_L11N/ GCLK5	E10	Differential pair with B0_IO23

Pin #	*Pin name*	*FPGA Pin name*	*FPGA Pin #*	*Description*
53	B0_I9	B0_IP_L13N/ GCLK9	B9	Differential pair with B0_I10 (input only)
54	B0_IO23	B0_IO_L11P/ GCLK4	D10	Differential pair with B0_IO22
55	GND			
56	GND			
57	B0_IO24	B0_IO_L12N/ GCLK7	A10	Differential pair with B0_IO25
58	B0_I7	B0_IP_L10N	G10	Differential pair with B0_I8 (input only)
59	B0_IO25	B0_IO_L12P/ GCLK6	B10	Differential pair with B0_IO24
60	B0_I8	B0_IP_L10P	F10	Differential pair with B0_I7 (input only)
61	GND			
62	GND			
63	B0_IO21	B0_IO_L09P	C11	Differential pair with B0_IO20
64	B0_I6	B0_IP_L07P	C12	Differential pair with B0_I5 (input only)
65	B0_IO20	B0_IO_L09N	D11	Differential pair with B0_IO21
66	B0_I5	B0_IP_L07N	D12	Differential pair with B0_I6 (input only)
67	GND			
68	GND			
69	B0_IO14	B0_IO_L05N/ VREF	B13	Differential pair with B0_IO15
70	B0_IO19	B0_IO_L08P	E11	Differential pair with B0_IO18
71	B0_IO15	B0_IO_L05P	A13	Differential pair with B0_IO14
72	B0_IO18	B0_IO_L08N	F11	Differential pair with B0_IO19
73	GND			
74	GND			
75	B0_IO12	B0_IO_L04N	A14	Differential pair with B0_IO13
76	B0_IO16	B0_IO_L06N	E12	Differential pair with B0_IO17
77	B0_IO13	B0_IO_L04P	B14	Differential pair with B0_IO12
78	B0_IO17	B0_IO_L06N	F12	Differential pair with B0_IO16
79	GND			
80	GND			
81	B0_I3	B0_IP_L02N	A15	Differential pair with B0_I4 (input only)
82	B0_IO10	B0_IO_L03N/ VREF	C14	Differential pair with B0_IO11
83	B0_I4	B0_IP_L02P	B15	Differential pair with B0_I3 (input only)
84	B0_IO11	B0_IO_L03P	D14	Differential pair with B0_IO10
85	GND			
86	GND			
87	B0_IO8	B0_IO_L01N	A16	Differential pair with B0_IO9
88	B3_IO0	B3_IO_L24P	T2	Bank 3, IO
89	B0_IO9	B0_IO_L01P	B16	Differential pair with B0_IO8
90	B0_IO6	B0_IO7	G9	

Pin #	Pin name	FPGA Pin name	FPGA Pin #	Description
91	GND			
92	B0_IO4	B0_IP_IO5	D13	
93	B0_IO7	B0_IP_IO7/ VREF	B11	
94	B0_IO2	B0_IO3	A11	
95	B0_IO5	B0_IO6	E13	
96	B0_IO0	B0_IP_IO1	A7	
97	B0_IO3	B0_IO4	C4	
98	B0_I2	B0_IP11	C15	Bank 0, input only
99	B0_IO1	B0_IO2	A8	
100	B0_I1	B0_NC_IO_ IP10	A12	Bank 0, input only
101	GND			
102	B0_I0	B0_IP9	A3	Bank 0, input only
103	GND			
104	GND			
105	GND			
106	GND			
107	GND			
108	GND			
109	2.5V			2.5V from module supply
110	2.5V			2.5V from module supply
111	2.5V			2.5V from module supply
112	2.5V			2.5V from module supply
113	2.5V			2.5V from module supply
114	2.5V			2.5V from module supply
115	VCC_0	VCC0		IO supply for bank 0
116	VCC_0	VCC0		IO supply for bank 0
117	VCC_0	VCC0		IO supply for bank 0
118	VCC_0	VCC0		IO supply for bank 0
119	VCC_0	VCC0		IO supply for bank 0
120	VCC_0	VCC0		IO supply for bank 0

Table 2: J1 connector pin out

Pin #	Pin name	FPGA Pin name	FPGA Pin #	Description
1	GND			
2	3.3V			3.3V supply to module
3	GND			
4	3.3V			3.3V supply to module
5	GND			
6	3.3V			3.3V supply to module

Pin #	*Pin name*	*FPGA Pin name*	*FPGA Pin #*	*Description*
7	B2_IO0	B2_IO1	P9	
8	B2_IO1	B2_IO2	R11	
9	B2_IO2	B2_IP_IO3	U6	
10	B2_IO3	B2_IP_IO4	U13	
11	B2_IO4	B2_NC_IO5	V7	
12	B2_IO5	B2_IO8/ VREF	T15	
13	B2_IO6	B2_IO9/ VREF	U5	
14	B2_IO7	B2_IO_L03P/ DOUT/BUSY	U4	
15	B2_IO8	B2_IO_L04N	T5	
16	B2_IO9	B2_IO_L04P	R5	
17	B2_IO10	B2_IO_L05N	P6	
18	B2_IO11	B2_IO_L05P	R6	
19	GND			
20	3.3V			3.3V supply to module
21	B2_IO12	B2_IO_NC_L 06N/VREF	V6	
22	B2_IO13	B2_NC_IO_L 06P	V5	
23	B2_IO14	B2_IO_L07N	P7	
24	B2_IO15	B2_IO_L07P	N7	
25	B2_IO16	B2_IO_L09N	N8	
26	B2_IO17	B2_IO_L09P	P8	
27	B2_IO18	B2_IO_L10N	T8	
28	B2_IO19	B2_IO_L10P	R8	
29	B2_IO20	B2_IO_l18N	N11	
30	B2_IO21	B2_IO_l18P	P11	
31	B2_IO22	B2_IO_L19N/ VREF	V13	
32	B2_IO23	B2_IO_L19P	V12	
33	GND			
34	3.3V			3.3V supply to module
35	B2_IO24	B2_IO_L20N	R12	
36	B2_IO25	B2_IO_L20P	T12	
37	B2_IO26	B2_NC_IO_L 21N	P12	
38	B2_IO27	B2_NC_IO_L 21P	N12	
39	B2_I0	B2_IP10	V2	Bank 2, input only
40	B2_I1	B2_IP11	V16	Bank 2, input only
41	B2_I2	B2_IP_L02N	V3	Bank 2, input only
42	B2_I3	B2_IP_L02P	V4	Bank 2, input only

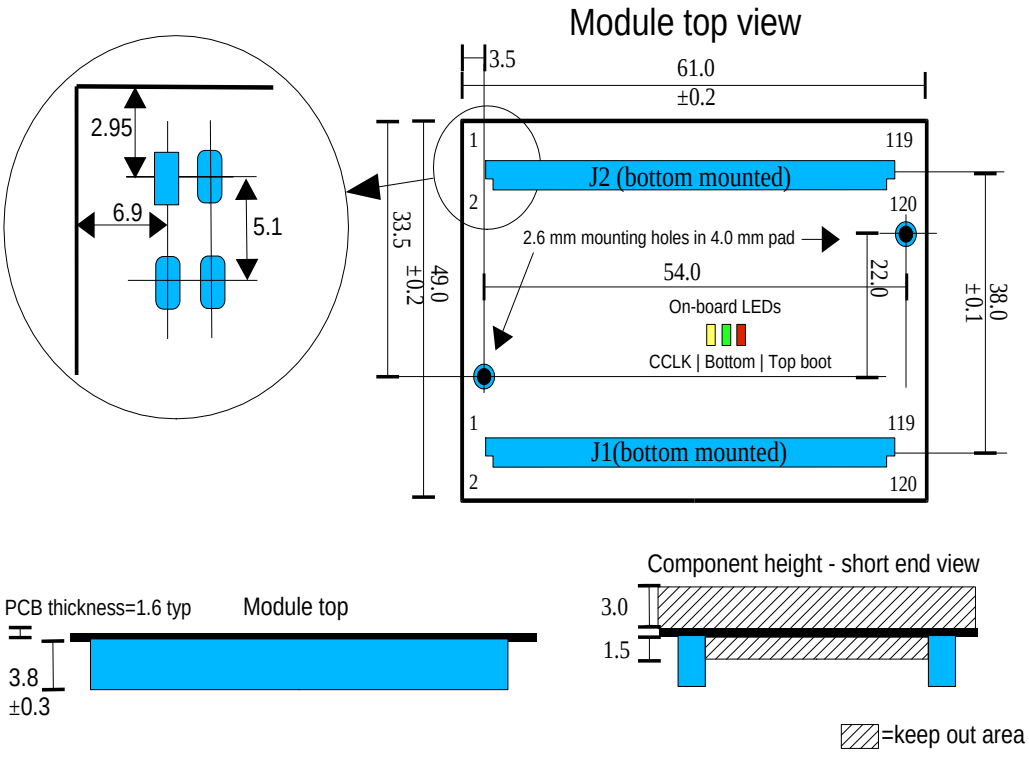
Pin #	*Pin name*	*FPGA Pin name*	*FPGA Pin #*	*Description*
43	B2_I4	B2_IP_L08N	R7	Bank 2, input only
44	B2_I5	B2_IP_L08P	T7	Bank 2, input only
45	B2_I6	B2_IP_L11N/ VREF	V8	Bank 2, input only
46	B2_I7	B2_IP_L11P	U8	Bank 2, input only
47	GND			
48	3.3V			3.3V supply to module
49	B2_I8	B2_IP_L14P/ RDWR_B/ GCLK0	U10	Bank 2, input only
50	B2_I9	B2_IP_L17N	U11	Bank 2, input only
51	B2_I10	B2_IP_L17P	T11	Bank 2, input only
52	B2_I11	B2_IP_L23N	U14	Bank 2, input only
53	B2_I12	B2_IP_L23P	V14	Bank 2, input only
54	B1_IO0	B1_NC_IO1	P16	
55	B1_IO1	B1_NC_IO_IP_L04N	N14	
56	B1_IO2	B1_NC_IO_IP_L04P	N15	
57	B1_IO3	B1_IO_L05N/ VREF	M13	
58	B1_IO4	B1_IO_L18N	G16	
59	B1_IO5	B1_IO_L18P	G15	
60	B1_IO6	B1_IO_L19N	F17	
61	GND			
62	3.3V			3.3V supply to module
63	B1_IO7	B1_IO_L19P	F18	
64	B1_IO8	B1_IO_L20N	G13	
65	B1_IO9	B1_IO_L20P	G14	
66	B1_IO10	B1_IO_L21N	F14	
67	B1_IO11	B1_IO_L21P	F15	
68	B1_IO12	B1_NC_IO_L22N	E16	
69	B1_IO13	B1_IO_L22P	E15	
70	B1_I1	B1_IO_IP2	E17	Bank 1, input only
71	B1_I2	B1_IP3	E18	Bank 1, input only
72	B1_I0	B1_IP1	B18	Bank 1, input only
73	B1_I4	B1_IP5	H13	Bank 1, input only
74	B1_I3	B1_IP4	G18	Bank 1, input only
75	GND			
76	3.3V			3.3V supply to module
77	B1_I6	B1_IP7	K18	Bank 1, input only
78	B1_I5	B1_IP6	K17	Bank 1, input only
79	B1_I8	B1_IP9	L14	Bank 1, input only

Pin #	*Pin name*	*FPGA Pin name*	*FPGA Pin #*	*Description*
80	B1_I7	B1_IP8	L13	Bank 1, input only
81	B1_I10	B1_IO_IP11	P15	Bank 1, input only
82	B1_I9	B1_IP10	N17	Bank 1, input only
83	B1_I12	B1_IP13/ VREF	D18	Bank 1, input only
84	B1_I11	B1_IP12	R17	Bank 1, input only
85	1.2V			1.2V from module supply
86	B1_I13	B1_IP14/ VREF	H18	Bank 1, input only
87	1.2V			1.2V from module supply
88	1.2V			1.2V from module supply
89	GND			
90	3.3V			3.3V supply to module
91	WD_TRIG	B2_IO_L03N MOSI/ CSI_B	T4	Watch-dog trigger output, configuration chip-select input, pulled down to GND by 10Kohm resistor
92	3.3V			3.3V supply to module
93	WE#	B1_IO_L23P/ HDC	D17	Common WE# signal to SRAM and FLASH
94	1.2V			1.2 V supply from module supply
95	D0	B2_IO_L16N/ DIN/D0	N10	Config. stream data, D0 of SRAM and FLASH
96	D1	B2_IO_L15N/ D1/GCLK3	P10	Config. stream data, D1 of SRAM and FLASH
97	D2	B2_IO_L15P/ D2/GCLK2	R10	Config. stream data, D2 of SRAM and FLASH
98	D3	B2_IO_L13N/ D3/GCLK15	V9	Config. stream data, D3 of SRAM and FLASH
99	D4	B2_IO_ L13P/D4/ GCLK14	U9	Config. stream data, D4 of SRAM and FLASH
100	D5	B2_IO6/D5	R9	Config. stream data, D5 of SRAM and FLASH
101	D6	B2_IO_L12N/ D6/GCLK13	M9	Config. stream data, D6 of SRAM and FLASH
102	D7	B2_IO_L12P/ D7/GCLK12	N9	Config. stream data, D7 of SRAM and FLASH
103	PROG_B	PROG_B	V17	FPGA reconfig pin, watch-dog output via 332 ohm resistor. Pulled to 2.5V via 4.75Kohm resistor
104	3.3V			3.3V supply to module
105	INIT_B	B2_IO_L01N/ INIT_B	T3	INIT_B configuration pin. Pulled to 3.3V using a 4.75Kohm resistor. User IO after configuration.
106	VBAT			3V Backup voltage for SRAM data retention
107	CSO_B	B2_IO_L01P CSO_B	U3	Configuration CS# output. User IO after configuration.
108	VBACKUP			VBAT/3.3V backup power output from MAX6362P (pin 5, ”OUT”)

Pin #	Pin name	FPGA Pin name	FPGA Pin #	Description
109	CCLK	B2_IO_L26N/ CCLK	U16	Configuration clock output. Yellow LED connected to 3.3V. 50 ohm series termination at FPGA.
110	DONE	DONE	B1	Configuration DONE . Pulled to 2.5V using a 332 ohm resistor.
111	TCK	TCK	A17	JTAG TCK (2.5V levels)
112	TDO	TDO	C16	JTAG TDO (2.5V levels)
113	TMS	TMS	D15	JTAG TMS (2.5V levels)
114	TDI	TDI	A2	JTAG TDI (2.5V levels)
115	GND			
116	3.3V			3.3V supply to module
117	GND			
118	3.3V			3.3V supply to module
119	GND			
120	3.3V			3.3V supply to module

The prefix B0_ indicates a FPGA bank-1 signal. Bank-0's VCCO pins are available on con. J2
The prefix B1_ indicates a FPGA bank-1 signal. Bank-1's VCCO pins are connected to 3.3V
The prefix B2_ indicates a FPGA bank-2 signal. Bank-2's VCCO pins are connected to 3.3V
The prefix B3_ indicates a FPGA bank-3 signal. Bank-3's VCCO pins are connected to 2.5V

Physical dimensions (mm)



Connector type: JAE KX15-120K2DE
Mates with: JAE KX14-120Kxxx

All dimensions are in mm

Absolute Maximum Ratings

Symbol	*Description*		*Min*	*Max*	*Unit*
V_{3V3}	External 3.3V supply to module		-0.5	3.75	V
V_{bat}	Backup supply for SRAM data retention		-0.5	3.8	V
V_{CCO}	FPGA output driver supply voltage		-0.5	V_{CCO}+0.5	V
V_{IN}	Voltage applied to bidirectional FPGA I/O pins as well as unidirectional input and output pins.(3) If present,driver is put in a high-impedance state.	V_{CCO}≤3.0	-0.5	V_{CCO}+0.5	V
		V_{CCO}<3.0	-0.3	3.75	V
T_{st}	Storage Temperature		-65	125	C°
T_{opc}	Operating temperature (commercial grade)		0	70	C°
T_{opi}	Operating temperature (Industrial grade)		-40	85	C°

DC Characteristics

Symbol	*Description*	*Min*	*Typ*	*Max*	*Unit*
V_{3V3}	External 3.3V supply to module	3.135	3.30	3.465	V
V_{2V5}	2.5V output from module		2.50		V
V_{1V25}	1.25V output from module	1.22	1.25	1.28	V
$I_{3V3,config}$	Configuration current consumption[1]		160		mA
$I_{3V3,active}$	Active current consumption[2]		310		mA
$P_{3V3,active}$	Active power consumption[2]		1,0		W
$I_{out,2V5}$	2.5 V supply output current			1.8	A
$I_{out,1V25}$	1.25 V supply output current			370	mA
I_{stdby}	SRAM standby current (Vbat=3.0V)		1.5	12	uA

[1] FPGA is reading configuration from flash (XC3S1600FGG320-5)
[2] Default FPGA image (DDR SDRAM @ 150 MHz being tested by a microblaze @ 75 MHz)

Ordering Information

Order code structure:

MPL3E-XXXX-YY-ZZ-QQQ-PPP

XXXX = FPGA type : 1200 for XC3S1200FGG320, 1600 for XC3S1600FGG320

YY = FPGA speed grade and temp. range: 4C, 5C, 4I (C=commercial, I=ind. temp. range)

ZZ = SRAM size in Mbits (always x16 organisation, industrial range):
00 (=not mounted), 01, 02, 04, 08, 16, 32 Mbits

QQQ = FLASH size in Mbits (always x16 organisation, industrial range): 128, 256, 512 Mbits

PPP = DDR1 DRAM size in Mbits (always x16 organisation): 128, 256, 512 Mbits

Preferred types:

MPL3E-1600-5C-01-256-512

MPL3E-1200-5C-01-128-512