XPS SD Card Interface

XPS_SD_IF_V1_00_a_PB **Product Brief**

Introduction

The XPS_SD_IF_V1_00_a IP core contains all the functions needed to interface a SD card to the PLB bus. The core allows software to efficiently execute send commands and receive responses to/from the SD card command interface while at the same time performing data transfers over the 1 or 4 bit data interface.

Programming is simplified by the built-in command request/response state machine and command CRC generation/checking blocks built into the core. This allows

Features

- Supports PLBv4.6 bus
- Optional PLB bus master DMA function for high speed transfer and CPU offloading
- Autonomous SD command execution with CRC generation and checking
- Data channel supports 1 or 4 bit interfaces and hardware CRC generation and checking
- Optional high performance DMA channel using PLB master port
- Programmable SD clock rates
- SD clock stopping for power reduction
- GPIO bits for card detection and write protection detection
- Supports SDHC commands
- MMC compatible

Core short specs.	
Supported Device Family	Spartan-3 Spartan-6 Virtex-4 Virtex-5 Virtex-6
Core Version	V1_00_a
Resource utilization	
Slices	
Block RAMs	
Special Features	none
Core deliveries	
Documentation	Data Sheet
Design Files	VHDL & Net list
Constraints File	N/A
Verification	On request
Instantiation Template	N/A
Ref. Design & Application Notes	N/A
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 11.2 or later
Verification	Xilinx BFL tool set
Simulation	Modelsim SE/PE 6.5 or later
Synthesis	XST
Support	
Provided by Morphologic ApS	

1. Functional Overview

The SD card interface core provides an interface between the relatively complex SD card protocol and the PLB bus/host controller. The controller simplify host operations by providing the following basic functions:

- State machine controlled command transmit and response sequencing
- Command CRC generation/checking in hardware
- Automatic data sector read and write operations with programme sector count
- Data CRC generation/checking in hardware
- 1 to 8 bit serialisation/deserialisation for command interface
- 1 / 4 bit to 32-bit data mux / demuxing for data interface
- Automatic data pausing when writing/erasing sectors
- Optional master PLB bus DMA controller for autonomous high speed data transfers
- GPIO bits for card detection, write protection state and card power on/off control.
- Programmable SD clock rate, from PLB bus clock/2 to PLB bus clock/256
- Interrupt generation for SD command completion
- Interrupt generation for SD data transfer completion (only for DMA interface)

Below is shown a block diagram of the SD interface core.

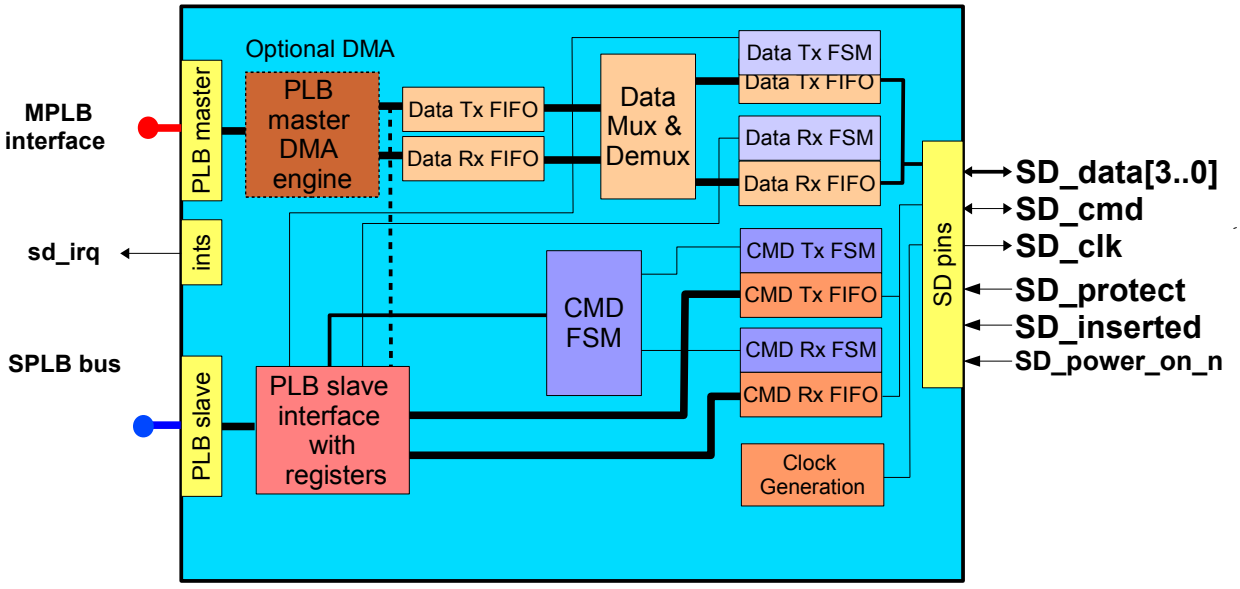

Fig 1. XPS_GRAPHICS_ENGINE IP block diagram.