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XPS Video and LCD Controller (v2.00b)

Introduction

The XPS_LCD_CTRL_V2_00_a IP core is a video and LCD controller that interfaces to a PLB V4.6 bus for reading video data and for register access. The core can control both passive and active (TFT) LCD displays as well as provide video data and timing for VGA and DVI interfaced displays. The IP core is intended for Xilinx based embedded FPGA designs.

Features

- Supports PLBv4.6 bus
- PLB bus master port width of 32 , 64 or 128 bits
- Selectable pixel FIFO depths of 256, 512 or 1024 words.
- Controls both passive and active LCD displays
- Passive displays can have 4096 colours using random frame rate modulation.
- Controls VGA monitors
- Includes optional PWM and GPIO channels for back light, contrast and display on/off control
- Frame synchronous base address reload to allow gaming displays.
- Frame interrupt signal for software synchronisation.
- Supports from 1 to 32 bits per pixel resolution
- Supports high-resolution display modes
- Separate pixel and system bus clocks
- Configurable small footprint core

Core short specs.	
Supported Device Family	Spartan-3 Spartan-6 Virtex-4 Virtex-5 Virtex-6
Core Version	V2_00_b
Resource utilization	
Slices	
Block RAMs	
Special Features	none
Core deliveries	
Documentation	Data Sheet
Design Files	VHDL & Netlist
Constraints File	N/A
Verification	On request
Instantiation Template	N/A
Ref. Design & Application Notes	N/A
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 11.2 or later
Verification	Xilinx BFL tool set
Simulation	Modelsim SE/PE 6.5 or later
Synthesis	XST
Support	
Provided by Morphologic ApS	

1. Functional Overview

The video controller enables the display of computer graphics on monitors, LCD panels and with the right video timing,- even television sets. Display data (pixels) are fetched from a PLB slave (typically a memory controller) , pushed into a FIFO and then read out from the FIFO and sliced up into the configured number of bits per pixel. The data for each pixel is then sent out on the output port one pixel at a time at the pixel clock rate. For passive LCD display modes, Frame Rate Modulation (FRM) is used to generate up to 16 shades of colours/white and for these modes a pixel clock is needed that is 16 times the LCD pixel clock rate. For active LCD displays and LCD monitors, this FRM is built into the screen logic and the display only needs N bits per colour to indicate which shade is displayed on the screen.

The video controller also generates the horizontal and vertical synchronization signals/clock needed for the display. The video timing is software programmable to suit most display and to be able to change screen size/position. The number of bits per pixel and video mode is however only configurable using generic parameters used at synthesis time. This keeps the size of the core footprint down to a minimum.

The parallel video data can be sent to:

- Directly to a LCD display module with parallel interface.
- An internal serialization core with LVDS output (for LCD display modules)
- An external video DAC chip with parallel inputs (for analog computer monitors)
- An external DVI chip via a DDR interface helper core (for computer monitors with DVI input)

Display data formats include, 8 bit packed formats used in passive LCD modules, where typically 4 pixels are packed in 3 consecutive bytes (colour modules) or 8 pixels in one byte (monochrome modules). FRM modes exist where the generated colour components are modulated to generate 16 shades of each basic colour, resulting in a total of 4096 colours.

Display timing is software programmable allowing for very flexible timing to suit various display requirements and timing standards such as those defined by VESA. Below is a shown a block diagram of the IP core. The dotted elements are optional., which can be selected at synthesis time using generic parameters.