Morphologic
Embedded FPGA Solutions
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XPS Graphics Engine (v2.00a)

Introduction

The XPS_GRAPHICS_ENGINE_V2_00_a IP core is 2D graphics rendering engine that interfaces to a PLB V4.6 bus for transfer of image data (master attachment) and for register access (slave attachment). The graphics engine uses a combination of dedicated graphics acceleration logic, a small footprint coprocessor and a PLB bus master attachment to render graphics. Using a command FIFO, commands containing instructions for rendering graphics primitives can be written by the host CPU, which will then be executed by the engine while the host CPU can continue with other tasks. Special hardware blocks accelerate plotting of single pixels as well as bit block transfers. The programmable co-processor reads commands from the command FIFO and configures the dedicated hardware for drawing pixels and performing bit block transfers (bitblt). The coprocessor program is preloaded with the standard software, but it can be reloaded via the control registers. The IP core is intended for Xilinx based embedded FPGA designs.

Features

- Supports PLBv4.6 bus
- Accelerates line and pixel plot operations.
- Accelerates bit block transfer operations.
- Support background masking and alpha blending.
- Small footprint due to optimisation of the combination of hardware and micro coded operations.
- Upgradeable/extensible microcode via user port
- Configurable small footprint core
- Supports 16 bits/pixel graphics mode.

Core short specs.	
Supported Device Family	Spartan-3 Spartan-6 Virtex-4 Virtex-5 Virtex-6
Core Version	V2_00_a
Resource utilization	
Slices	
Block RAMs	
Special Features	none
Core deliveries	
Documentation	Data Sheet
Design Files	VHDL & Net list
Constraints File	N/A
Verification	On request
Instantiation Template	N/A
Ref. Design & Application Notes	N/A
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 11.2 or later
Verification	Xilinx BFL tool set
Simulation	Modelsim SE/PE 6.5 or later
Synthesis	XST
Support	
Provided by Morphologic ApS	

1. Functional Overview

The core consist of two hardware blocks dedicated to pixel plotting and bit block transfers. The hardware engine request bus operations to the PLB bus master DMA engine and feeds/takes pixel data using small read and write data FIFOs. Bit block transfer operations are always executed using 8x32bit transfers.

The core also contains a small footprint graphics engine CPU (GECPU), which receives commands and command parameters over the command FIFO. The GECPU breaks the graphics operations into bit plot and bitblt primitive operations and configures the relevant hardware block to execute the sub-operations needed to complete the graphic command. The GECPU can utilize the time it takes for the hardware engines and bus interface to complete the operation, to prepare the next primitive operation. This split between hardware and software reduces the amount of logic needed while providing good performance and flexibility.

The GECPU uses a single 18Kbit block RAM to store it's instructions. The block RAM can be accessed indirectly using the core control registers so that it's contents can be changed. The block RAM is preloaded with the default software upon configuration of the FPGA.

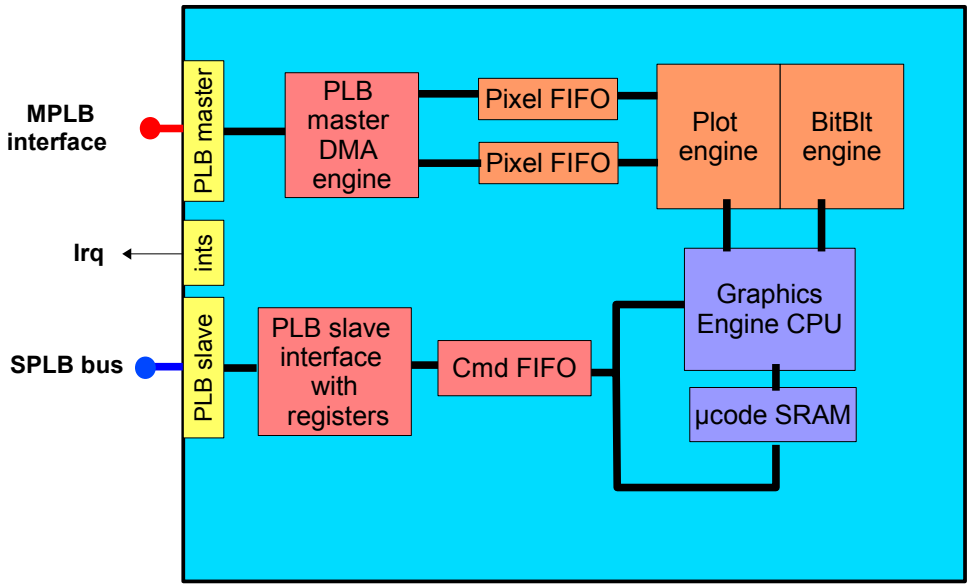

Fig 1. XPS_GRAPHICS_ENGINE IP block diagram.