OPB Keyboard Scanner

The OPB_KEYSCAN IP core is a core used for interfacing a matrix keyboard to the OPB bus. The core will scan the keyboard, detect and debounce any keys pressed and store a scankode corresponding to the key pressed. The IP core eliminates the need for the host CPU to scan the keyboard in software, reducing valuable interrupt time and CPU resources while simplifying the design.

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Product key features:

The OPB_KEYSCAN IP cores simplifies the task of attaching a keyboard to an embedded FPGA system. The core can be configured to scan matrix keyboards with a matrix of up to 128 keys. The number of rows (outputs) and columns (input) are programmable. When ever a key is pressed or released the scancode corresponding to the key is stored in a 2-byte deep FIFO. Keeping a key depressed will – after a selectable delay, result in the key's scancode to be returned repeatedly with a selectable delay. Repeating action can be enabled/disabled via a generic option to reduce the amount of logic used by the core. The scancode consisting of a single byte, will have it's msb set if the key is pressed and reset when it's released. An interrupt can be enabled for either a keypress and/or a key release. An optional extra FIFO can be added to the 2-byte fifo, allowing up to 16 extra scancodes to be buffered. The core can handle that one key is pressed while scanning continues to detect another keypress. This allows the usage of shift functions.